Clean copy of the allowed claims

1. A system to provide power in a specified voltage range to an integrated circuit comprising:

a power delivery network characterized by a response function; and

a device to draw power from the network, the device including:

a first shift register to store values representing a sequence of current amplitudes drawn by the device on successive clock cycles;

an adder having inputs weighted to reflect the response function of the power delivery network, the adder to determine a weighted sum of the sequence of current amplitudes to estimate a voltage provided to the device;

a voltage comparator to compare the estimated voltage to a voltage threshold; and

a throttle unit to adjust operation of the device responsive to the estimated voltage reaching the voltage threshold.

2. (Deleted)

3. (deleted)

4. The system of claim 3, wherein the device is a processor that further comprises:

an execution pipeline including one or more units to process instructions;

a fetch unit to deliver instructions to the execution pipeline; and

a clock gating unit to control the delivery of power to the one or more units, responsive to use of the unit by a currently executing instruction.

5. The system of claim 4, wherein the throttle unit prevents the clock gating unit from gating off power to the one or more units, responsive to the estimated voltage exceeding an upper threshold voltage.

6. The system of claim 4, wherein the throttle unit signals the fetch unit to deliver instructions to the execution pipeline at a reduced rate, responsive to the estimated voltage falling below a lower threshold voltage.

7. The system of claim 1, wherein the response function of the power delivery network is represented by n response function amplitudes, and the weighted inputs of the adder comprises n inputs that are weighted proportionally to the n response function amplitudes.

8. The system of claim 1, wherein the response function of the power delivery network is represented by a set of recursion coefficients, and the weighted inputs of the adder are weighted proportionally to the recursion coefficients.

9. The system of claim 8, wherein the device further comprises a second shift register to track a sequence of estimated voltages provided by the adder and to feedback the sequence of estimated voltages to selected inputs of the adder.

10. The system of claim 9, wherein the recursion coefficients include a set of current coefficients and a set of voltage coefficients.

11. The system of claim 10, wherein adder inputs include first and second sets of inputs coupled to outputs of the first and second shift registers, the first set of inputs being weighted proportionally to the current coefficients and the second set of inputs being weighted proportionally to the voltage coefficients.

12. A system to provide power in a specified voltage range to an integrated circuit comprising:

a power delivery network characterized by a response function;

a processor core to execute instructions, the processor core to draw power from the network, responsive to the instructions it executes;

a monitor unit to estimate a voltage provided to the processor core, the monitor unit including:

a current computation unit to track a sequence of current values drawn by the processor core on successive clock cycles; and

a current to voltage computation unit to filter the sequence of current values according to the response function to provide an estimated voltage provided to the processor core;

a threshold comparator to determine if the estimated voltage is within a specified range; and

a throttle unit to adjust operation of the processor core responsive to the estimated voltage not being within the specified range.

13. (Deleted).

14. The system of claim 12, wherein the processor core includes multiple pipeline units that are selectively activated, responsive to one or more of the instructions, each of the multiple pipeline units having an associated gate unit to provide a current signal to the pipeline unit if the pipeline unit is activated on a given clock cycle.

15. The system of claim 14, wherein current computation unit includes a shift register having a sequence of entries to store current values for a sequence of clock cycles, the stored current values to represent a sum of current signals provided to the pipeline units on each of the clock cycles of the sequence.

16. The system of claim 12, wherein the current computation unit includes an adder to estimate current amplitudes drawn by the processor core on a sequence of m intervals and an m-entry shift register to store the estimated current amplitudes of m intervals.

17. The system of claim 16, wherein the current to voltage computation unit includes an adder having m inputs, each input being weighted according to the response function of the power delivery network, the adder to estimate the voltage provided to the

processor core as a weighted sum of the m current amplitudes provided by the m-entry shift register.

18. The system of claim 17, wherein the response function is an impulse function for the power delivery network and the m inputs of the adder are weighted proportionally to amplitudes of the impulse function at m intervals.

19. The system of claim 17, further comprising a p-entry shift register to store a sequence of p estimated voltages provided by the adder, and to feedback the p estimated voltages to inputs of the adder.

20. The system of claim 19, wherein the adder inputs coupled to the m-entry shift register are weighted proportionally to a first set of recursion coefficients derived from the response function of the power delivery network and the adder inputs coupled to the p-entry shift register are weighted proportionally to a second set of recursion coefficients derived from the response function.

21. An apparatus to estimate a voltage provided to a device in an integrated circuit comprising:

a shift register having n entries to store values representing current amplitudes on n successive intervals;

n weight units, each weight unit to scale a current amplitude value from a corresponding entry of the shift register;

an adder to sum the scaled current amplitudes from the weight units to provide an estimated voltage provided to the device.

22. The apparatus of claim 21, further comprising a second adder to sum current amplitudes from one or more circuits and to provide the sum to a first entry of the shift register, responsive to a clock signal.

23. The apparatus of claim 22, wherein each of the weight units stores a value representing a response function for a system in which the apparatus is to operate.

24. The apparatus of claim 23, wherein the adder includes p additional inputs and the apparatus further comprises a second shift register having p entries to store a sequence of estimated voltages and to feedback the estimated voltages to the p additional inputs of the adder, the estimated voltages being provided by the adder.

25. The apparatus of claim 23, wherein the n and p inputs of the adder are weighted according to current and voltage recursion coefficients derived from the response function.